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14. ABSTRACT
Black Forest Engineering's (BFE's) objective of the Phase I effort was to develop thermopile infrared detector linear arrays meeting the requirements of chemical and biological sensing such as Foster-Miller's Infrared Bio-Aerosol Threat Alert (IBATA) system. BFE's thermopile fabrication objective is to use materials and processes compatible with standard silicon based integrated circuit foundries in order to reduce cost. The fabrication of silicon-based thermopiles, differentially coupled with advanced BFE CMOS readout integrated circuitry (ROIC),

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Report Title

MEMS Based Thermopile Infrared Detector Array for Chemical and Biological Sensing

ABSTRACT

Black Forest Engineering's (BFE's) objective of the Phase I effort was to develop thermopile infrared detector linear arrays meeting the requirements of chemical and biological sensing such as Foster-Miller's Infrared Bio-Aerosol Threat Alert (IBATA) system. BFE's thermopile fabrication objective is to use materials and processes compatible with standard silicon based integrated circuit foundries in order to reduce cost. The fabrication of silicon-based thermopiles, differentially coupled with advanced BFE CMOS readout integrated circuitry (ROIC), will provide DOD with rugged, inexpensive, and high performance infrared sensing capabilities. The Phase I design objective was to implement a ? 64-channel linear array with 0.5 mm pitch and > 90% fill factor. The MEMs based LWIR (8-12 Jm) thermopile array will provide detectivity (D*) > 1 x 108 Jones, time constant < 35 msec and temperature coefficient of responsivity (TCR) < 0.04%/C. The thermopile resistance will be > 90 kOhms; compatible with BFE's low noise differential input circuitry. On Phase II the thermopile detector linear array can be fabricated and integrated with an existing BFE ROIC optimized for thermopile linear array readout.

List of papers submitted or published that acknowledge ARO support during this reporting period. List the papers, including journal references, in the following categories:

(a) Papers published in peer-reviewed journals (N/A for none)

Number of Papers published in peer-reviewed journals: 0.00

(b) Papers published in non-peer-reviewed journals or in conference proceedings (N/A for none)

Number of Papers published in non peer-reviewed journals: 0.00

(c) Presentations

Number of Presentations: 0.00

Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

Number of Non Peer-Reviewed Conference Proceeding publications (other than abstracts): 0

Peer-Reviewed Conference Proceeding publications (other than abstracts):

Number of Peer-Reviewed Conference Proceeding publications (other than abstracts): 0

(d) Manuscripts

Number of Manuscripts: 0.00

Patents Submitted

Patents Awarded

Awards

Graduate Students

NAME	PERCENT_SUPPORTED

FTE Equivalent:
Total Number:

Names of Post Doctorates

NAME	PERCENT_SUPPORTED

FTE Equivalent:
Total Number:

Names of Faculty Supported

NAME	PERCENT_SUPPORTED

FTE Equivalent:
Total Number:

Names of Under Graduate students supported

NAME	PERCENT_SUPPORTED

FTE Equivalent:
Total Number:

Student Metrics

This section only applies to graduating undergraduates supported by this agreement in this reporting period

The number of undergraduates funded by this agreement who graduated during this period:	0.00
The number of undergraduates funded by this agreement who graduated during this period with a degree in science, mathematics, engineering, or technology fields:.....	0.00
The number of undergraduates funded by your agreement who graduated during this period and will continue to pursue a graduate or Ph.D. degree in science, mathematics, engineering, or technology fields:.....	0.00
Number of graduating undergraduates who achieved a 3.5 GPA to 4.0 (4.0 max scale):	0.00
Number of graduating undergraduates funded by a DoD funded Center of Excellence grant for Education, Research and Engineering:	0.00
The number of undergraduates funded by your agreement who graduated during this period and intend to work for the Department of Defense	0.00
The number of undergraduates funded by your agreement who graduated during this period and will receive scholarships or fellowships for further studies in science, mathematics, engineering or technology fields:	0.00

Names of Personnel receiving masters degrees

NAME

Total Number:

Names of personnel receiving PHDs

NAME
Total Number:

Names of other research staff

NAME	PERCENT_SUPPORTED	
Hari Rajgopal	1.00	No
FTE Equivalent:	**1.00**	
Total Number:	**1**	

Sub Contractors (DD882)

Inventions (DD882)

Scientific Progress

The thermoelectric properties of n-SiC have been thoroughly studied through the characterization of the electrical resistivity, the Seebeck coefficient and the thermal conductivity of n-SiC thin film. The 0.93 ?m-thick, n-SiC thin film utilized in the thermoelectric flow sensor has an electrical resistivity of 9.94 m?-cm, with a negative temperature coefficient (TCR) between 685 ppm/°C to 701 ppm/°C. The effect of film thickness on the electrical resistivity of n-SiC thin films has also been studied. The resistivity of n-SiC film decreases by a factor of ~7, from 38 m?-cm for the 100 nm thick films to 5.4 m?-cm for the 1.78 ?m-thick films. The Seebeck coefficient is measured to be -10 ?V/K at room temperature, with a lateral thermal conductivity of 64 W/mK. The Seebeck coefficient increased to -20 ?V/K at 300°C.

Technology Transfer

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April 20, 2011

U. S. Army Research Office

RDRL-ROE-L

Attn: Dr. William Clark

P.O. Box 12211

Research Triangle Park, NC 27709-2211

Dear Dr. Clark,

Enclosed is a copy of the Final Report for topic A10a-T004 STTR contract number W911NF-10-C-0121, MEMS Based Thermopile Infrared Detector Array for Chemical and Biological Sensing. This report is submitted in fulfillment of CDRL 0001AF and summarizes work performed on the contract from 23 September 2010 – 22 March 2011.

If you have any questions regarding the report contact Stephen Van Duyne at 719-593-9501 ext 299 or Jim Gates at 760-730-9768

Sincerely,

Stephen Van Duyne

Enclosure

MEMS Based Thermopile Infrared Detector Array for Chemical and Biological Sensing

Black Forest Engineering, LLC

Army Phase I STTR – Contract Number W911NF-10-C-0121

0001AF 22 March 2011 – Final Report

20 April 2011

Principal Investigator: Dr. Stephen Gaalema

Results of the Phase I Work

Black Forest Engineering's (BFE's) objective of the Phase I effort was to develop thermopile infrared detector linear arrays meeting the requirements of chemical and biological sensing such as Foster-Miller's Infrared Bio-Aerosol Threat Alert (IBATA) system. BFE's thermopile fabrication objective is to use materials and processes compatible with standard silicon based integrated circuit foundries in order to reduce cost. The fabrication of silicon-based thermopiles, differentially coupled with advanced BFE CMOS readout integrated circuitry (ROIC), will provide DOD with rugged, inexpensive, and high performance infrared sensing capabilities. The Phase I design objective was to implement a ≥ 64-channel linear array with 0.5 mm pitch and > 90% fill factor. The MEMs based LWIR (8-12 µm) thermopile array will provide detectivity (D*) > 1 x 10^8 Jones, time constant < 35 msec and temperature coefficient of responsivity (TCR) < 0.04%/C. The thermopile resistance will be > 90 kΩ compatible with BFE's low noise differential input circuitry. On Phase II the thermopile detector linear array can be fabricated and integrated with an existing BFE ROIC optimized for thermopile linear array readout.

Today's high performance thermopiles linear arrays, using Bi-Te/Bi-Sb-Te thermocouples, are not affordable for low cost (< $1000) spectrometers. The lack of affordability is due in part to the fact that Bi-Te/Bi-Sb-Te is not compatible with conventional silicon-based semiconductor fabrication lines and detector arrays are processed in custom or dedicated process facilities. Thermopile infrared detectors processed in standard integrated circuit process facilities, combined with advanced CMOS readouts optimized for thermopile array readout will provide low-cost and high performance sensing capabilities for spectrometers.

BFE has identified eight advantages that justify the use of silicon-based semiconductors and integrated circuit (IC) processing in thermopile linear array fabrication:

1. Thermocouples made from silicon-based semiconductors offer a high Seebeck coefficient.

2. Silicon-based thermocouples demonstrate a low temperature coefficient of responsivity.

3. IC processing/miniaturization provides low thermal conductance and thermal capacity.

4. Absorber structures based on sub-wavelength resonant diffraction reduce thermal mass.

5. Suspension of the thermopile can be accomplished with CMOS processes.

6. IC processes provide large wafers and batch processing to lower fabrication cost.

7. On-silicon wafer dewar and window provides low cost, reliable and compact packaging.

8. Monolithic integration of the thermopile and (ROIC) on the same wafer is possible if desired.

Prior to the Phase I proposal BFE discussed the thermopile requirements with Foster-Miller (Ani Weling at QinetiQ North America). Figure 1 shows a Foster Miller's 1x64 thermopile array with pixel pitch of 500 µm and pixel height of 1500 µm.

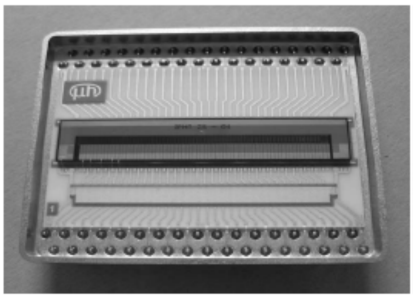

Figure 1. Foster-Miller 64 pixel linear thermopile array photograph

The specifications for the Foster-Miller thermopile array are compared in Table I to the BFE and STTR goals. BFE selected these design goals to first meet the STTR specifications and second obtain performance close to that desired by Foster-Miller (and their Bi-Te/Bi-Sb-Te based array processed in Europe).

Table I. BFE thermopile array STTR design goals compared to requirements

Array Property	Foster-Miller Value	BFE (STTR) Design Goal
Number of pixels	64	≥ 64
Operating wavelength	2-16 µm	2-16 µm (8-12 µm)
Pixel resistance	9 kΩ	> 90 kΩ (>90 kΩ)
Pixel width (dispersion)	450 µm	480 µm (> 90% fill factor)
Pixel height	1500 µm	1500 µm
Pixel pitch	500 µm	500 µm
Responsivity in vacuum	245 V/W	>245 V/W
D* (cmHz$^{1/2}$/W)in vacuum	1.6 x 10^{9}	>1.0 x 10^{9} (> 1 x 10^{8})
NEP (pW/Hz$^{1/2}$) in vacuum	200	<200
Response time (ms) in vacuum	150	< 35 (< 35)
Temperature coefficient resp.	Typically ~ 0.4%/K	< 0.04%/C (< 0.04%/C)
connections/thermopile	1 + 1 common	2/thermopile

The > 90 kΩ thermopile resistance was a STTR goal and is also compatible with the existing BFE ROIC. The responsivity thermal time constant in vacuum was designed for < 35 msec meeting STTR requirements. The baseline D* goal does not meet Foster-Miller requirements but the BFE (and STTR) thermal constant requirement is 35 msec vs. 150 msec. Thermopile arrays for Foster-Miller applications can use higher thermal isolation, increasing thermal time constant, then meeting Foster-Miller D* requirements due to higher responsivity. The BFE thermopile design uses two individual contacts per thermopile, whereas the Foster-Miller thermopile uses one unique thermopile contact and one array common. The BFE electronic chopper amplifier provides a doubling in responsivity and two samples per dwell time; this improves D* by 2$^{1/2}$ compared to an array common connection approach. The reduced TCR (temperature coefficient of responsivity) of <0.04%/K meets the STTR goal using silicon based

p and n semiconductors. This represents about 10x improvement compared to Bi-Te/Bi-Sb-Te thermocouples.

1. Thermocouple Material Considerations:

BFE and Case Western Reserve University investigated three different silicon-based materials for thermocouple fabrication. These materials are standard CMOS gate N+/ P+ doped poly silicon, N+ SiC/P+ poly-Si, and N+/P+ doped poly-SiGe.

1. Standard CMOS polysilicon (P+ and N+) for thermocouple/thermopile:

The standard CMOS polysilicon, used in a 180/250 nm CMOS process, is about 250 nm thick, doped at the same time as source/drain implant, resulting in N+ and P+ polysilicon of sheet resistance ~ 300 Ω/□ (doping dose ~ 7 x 10^{15}/cm^2). Most CMOS processes allow a lighter doped P+ polysilicon for resistors (~ 1000 Ω/□). The goal of the BFE CMOS process thermopile fabrication is to use standard processes. The use of 1000 Ω/□ P+ polysilicon will not result in significant thermocouple performance; however use of lighter doped N-type polysilicon may result in improved thermocouple performance (higher Seebeck coefficient). This may be an option in production at some CMOS foundries.

A unique design feature of the BFE CMOS foundry based process is the use of silicide (polycide) to make a low resistance contact between the N+ and P- polysilicon. The low resistance polycide connection is shown in figure 2. In this figure the N+ and P+ polysilicon thermocouples legs are shown (blue and pink) where the CMOS standard low resistance polysilicon interconnect is shown in grey.

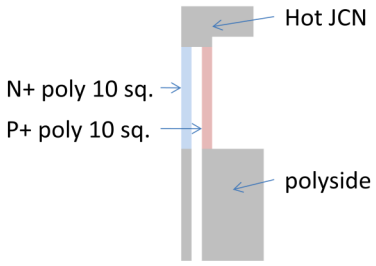

Figure 2. BFE uses polycide to make low resistance N+/P+ polysilicon interconnect

The thermocouples are arranged in the x-direction to make an 8 element thermopile as shown in figure 3. The dark blue regions are used to etch down through the oxide and underlying silicon to suspend the thermopile at the end of the CMOS process. In this case each thermocouple has about 6 kΩ resistance (20 squares total length at 300 Ω/□).

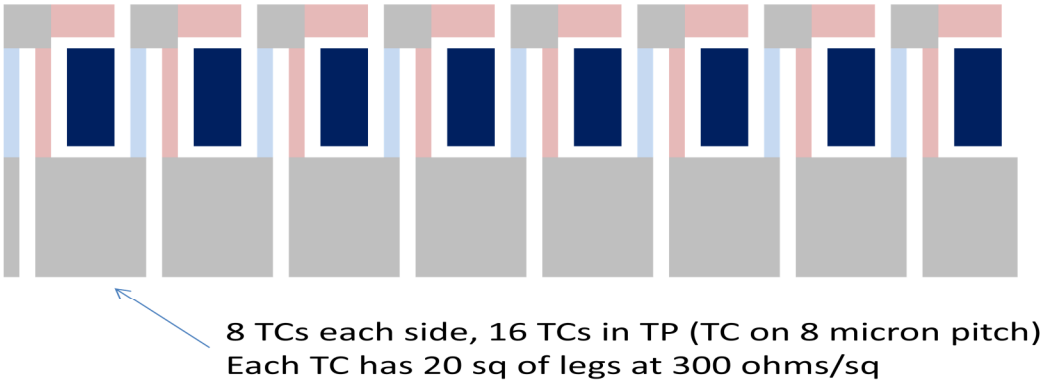

Figure 3. Thermocouples arrayed in the x-direction

A complete thermopile is shown in figure 4. In this case nine thermocouples are on the bottom and nine thermocouples on the top. The thermocouples are interconnected by polycide (~10 Ω/□). The central area has a P+ polysilicon grid covered by silicon dioxide to 1) absorb photons, 2) spread out the heat, and 3) provide diffractive tuned-resonance absorption. The pitch of the polysilicon mesh can be adjusted to optimize (tune) the absorption wavelength in any given pixel by design. This thermopile (with tuning modification) can be arrayed in the x-direction to make a linear array. While not shown, the pixel spacing can be reduced to less than 20 µm for a high fill factor.

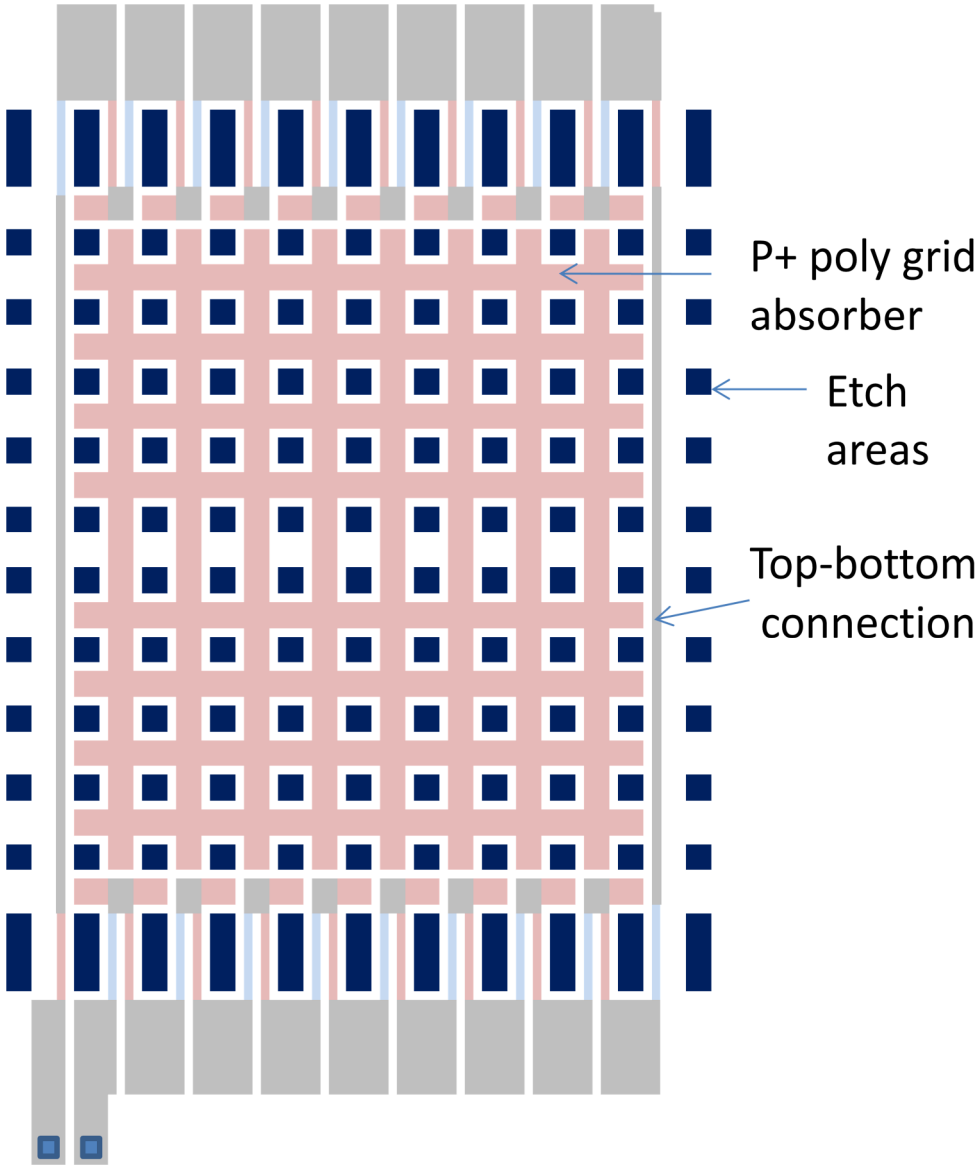

Figure 4. Complete thermopile with eighteen thermocouples (just an example)

BFE used published N+ and P+ polysilicon thermoelectric properties to model the thermopile performance[1]. The thermocouple figure of merit is a function of the Seebeck coefficient, electrical resistivity, thermal conductivity and temperature. The thermal conductivity of doped polysilicon (at 300K) is shown in figure 5. The heavier doping dose (7E15/cm^2) obtained by ion implantation is typical of that used in P and N-channel transistors (with boron and phosphorous respectively) in a 180 nm CMOS process. A lighter boron doped polysilicon (~2E15/cm^2) is also available in the 180 nm CMOS as a resistor layer (~ 1000 ohms/□). Figure 6 shows polysilicon electrical resistivity versus doping. This poly-Si thermal conductivity and electrical resistivity was used in the thermopile leg optimization.

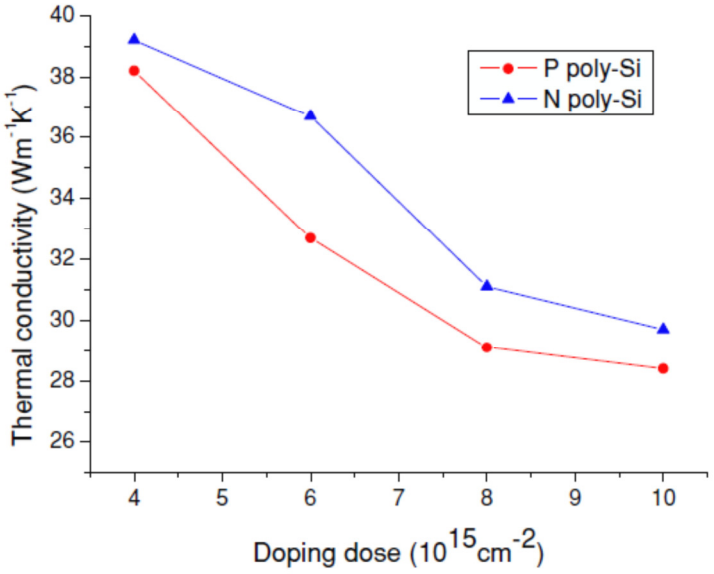

Figure 5. Thermal conductivity at 300K of doped polysilicon [ref 1]

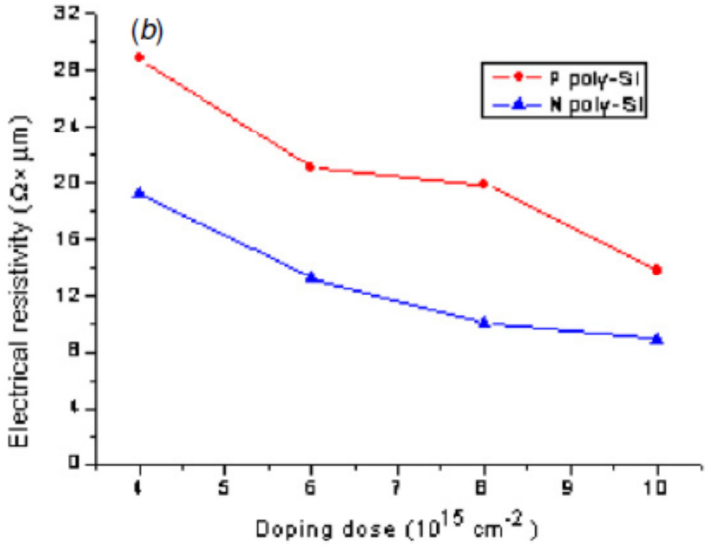

Figure 6. Electrical resistivity at 300K of doped polysilicon [ref 1]

The Seebeck coefficient is also a function of polysilicon doping level as shown in figure 7. The Seebeck coefficient, electrical resistivity and thermal conductivity of doped polysilicon can be used to calculate the figure of merit (ZT) for polysilicon as shown in figure 8. Unfortunately in a standard 180/250 nm CMOS process a lightly doped n-type polysilicon is not available. It may be possible to request an additional implant (using the polysilicon resistor layer), and if so, using less doping in the n-type polysilicon would improve the n-leg figure of merit (see figure 8). Low

doped concentration N- poly-Si may exhibit high contact resistance (even with silicide/polycide contacts) so a higher N+ ion implant doping can be added to the contact regions (using the standard NFET N+ implants).

BFE will baseline use of standard 7E15/cm^2 N+ and P+ ion implant doses in both legs of the polysilicon thermocouples. BFE could further optimize the thermopile performance by modification of the CMOS foundry process (different poly-Si resistor implant used for the n- leg) and this can be done in production where BFE procures the entire lot and can make some minor implant modification to poly-Si resistor implants. The standard CMOS process allows the thermopile to be processed alongside the ROIC and interconnected without use of wire bonds. This approach will allow smaller pixel pitch, no wire bonds for thermopile connection and for some applications area arrays for time delay integration (scanned/push-broom applications).

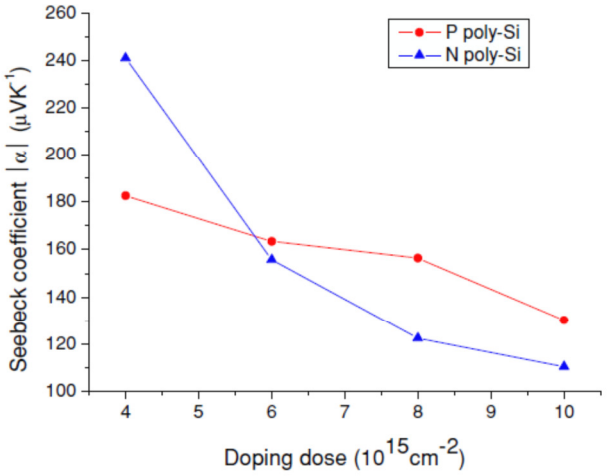

Figure 7. Seebeck coefficient at 300K of doped polysilicon [ref 1]

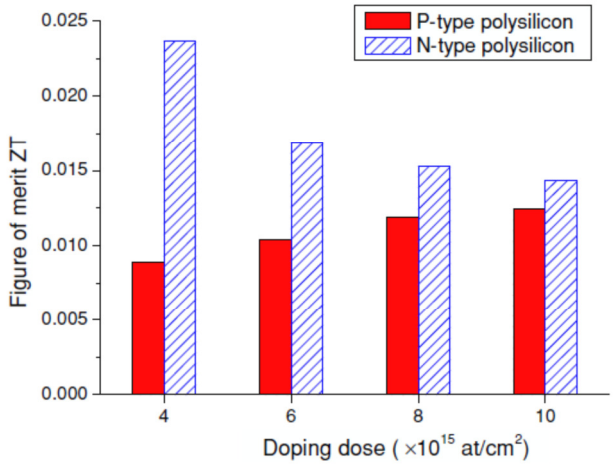

Figure 8. Figure of merit of doped polysilicon at 300K [ref 1]

Reference 1: for figures 5-8 is Jin Xie, et. al., "Characterization of heavily doped polysilicon films for CMOS-MEMS thermoelectric power generators", J. Micromech. Microeng. 19 (2009).

The Bi-Sb based thermocouples have relatively large temperature coefficient of responsivity (TCR). The poly-Si thermopiles have TCR ~ -0.04 % / K that is 8 times lower than that for Bi-Sb based thermopiles. Figure 9 show a TCR comparison of BiSb and poly-Si based thermocouples. The poly-Si has the capability of coming close to or meeting the STTR TCR requirements. The low TCR is desired since calibration of an instrument with such a low TCR for the detector is much easier and requires less calibration steps.

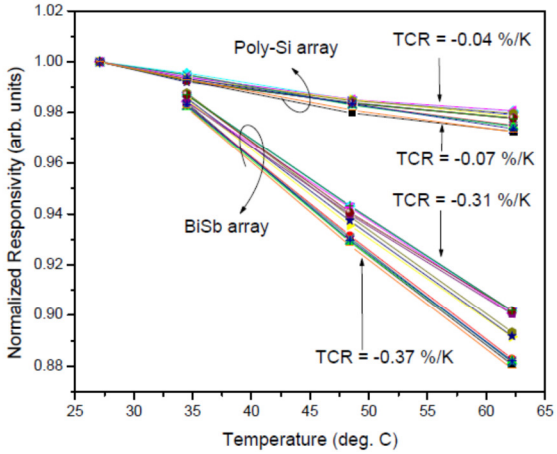

Figure 9. BiSi and poly-Si based thermopile TCR comparison
(from Dexter Research, SPIE Vol. 7680, April 2010)[ref2]

2. N+ SiC/P+ PolySi CMOS polysilicon thermocouple/thermopile:

BFE is teamed with CASE WESTERN on the STTR to develop high performance thermopiles (higher Z (figure of merit)). The materials being investigated are based on those available in a silicon process facility (CMOS or MEMS) but not necessarily available in a standard CMOS process run at this time. The thrust of this research is obtaining a high thermoelectric figure of merit and D* compared to doped polysilicon. The work with CASE was directed toward SiC (a MEMS material). The high Z material would most likely require a custom process at an IC or MEMs foundry and linear thermopile array wire bonded to the ROIC. BFE's baseline STTR approach is n-p polysilicon thermopiles (fabricated using the standard CMOS gate polysilicon) and fabrication of the linear array on the ROIC wafer using a CMOS process.

In prior published work by CASE, "THERMOELECTRIC CHARACTERISTICS OF N-TYPE POLYCRYSTALLINE SILICON CARBIDE AND COMPARISON WITH CONVENTIONAL THERMOPILES," IEEE Transducers Conference Proceedings, pp. 1861-1864, June 21-25, 2009[ref3], CASE reported on n-type SiC with a high Seebeck coefficient (~2 mV/K) but the thermal conductivity was also very high (360 W/mK) and about 10x the thermal conductivity of polysilicon (~ 30 W/mK). The poly-Si thermal conductivity is shown in figure 5. The high

Seebeck coefficient of SiC (α) significantly improves the figure of merit ZT (goes as α^2) so a 10x higher thermal conductivity of SiC compared to poly-Si, at first glance, seems not a problem.

The high Seebeck coefficient of n-type Si:C is desirable but the high thermal conductivity makes design of a thermopile with high thermal isolation difficult. In systems where the thermopile is vacuum packaged and the thermopile is designed to achieve near radiative limited performance, the Si:C thermal conductivity needs to be reduced. In semiconductors the thermal conductivity can be reduced by increase in doping concentration (see figure 5 as an example for poly-Si). On Phase I, BFE and CASE investigated increased doping concentration to reduce the thermal conductivity of SiC while hopefully maintain a high Seebeck coefficient and ZT. The increased n-type SiC doping might also reduce electrical contact resistance with Al-SiC contacts that was noticed as a problem in the prior CASE 2009 study (adds to thermopile resistance and creates excess Johnson noise).

The heavily-doped n-SiC studied on Phase I was doped with nitrogen to ~9×10^{20} atoms/cm^3. The doping concentration of n-poly-SiC in the CASE 2009 study was ~1 x 10^{20} atoms/cm^3. The electrical resistivity as a result increased doping did not change from the prior 2009 results. The CASE thermal conductivity measurement method, shown in figure 10, was utilized to determine the thermal conductivity of the 0.93 μm-thick n-SiC film with high doping.

The test structure has a n-SiC bridge suspended over a cavity. The bridge structure is used to minimize heat loss to the substrate and uniformly directs the heat conduction in only one direction along the bridge. One heater (also served as a thermistor) and two thermistors made of boron doped polysilicon (p-Si) were deposited on top of the n-SiC with 150 nm-thick of thermal oxide isolation in between. When constant current is applied across the heater, there is a thermal gradient generated between the heater and the thermistor. Thus, the thermal conductivity k can be calculated.

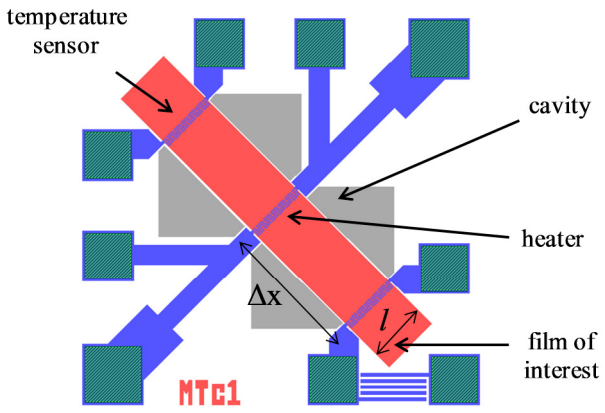

Figure 10. Thermal conductivity test method at CASE

The thermal conductivity of the Phase I highly doped n-SiC thin film was 64 $Wm^{-1}K^{-1}$. This is a significant reduction from the 2009 results (360 W/mK) but still ~2X that of polysilicon. The

electrical resistivity did not change much between the ~9 x 10^{20} and ~ 1 x 10^{20} doping level indicating that additional doping beyond 1 x 10^{20} atoms/cm^3 doping is not electrically active.

The next task, on Phase I, was to measure the Seebeck coefficient of the ~9×10^{20} atoms/cm^3 doped SiC. The CASE Seebeck test structure is depicted in figure 11. Each thermocouple comprises of one 15 µm-wide, 0.93 µm-thick n-SiC leg; and one 8 µm-wide, 300 nm-thick platinum leg (with 20 nm-thick of Ti as adhesion layer). Both elements are 750 µm long. There are a total of 16 thermocouples with 32 junctions connected together in series to create the thermopile. The temperature sensors are n-SiC thermistors, which can be used to measure the hot and cold junction temperatures via temperature coefficient thermometry. The cold junctions of the thermopile are contacting to the substrate, whereas the hot junctions are suspended over a cavity to enhance thermal isolation. Then, the ΔV and ΔT measured from the experiment can be used to calculate the Seebeck coefficient for Pt/SiC and the absolute Seebeck coefficient of n-SiC is obtained by using the known Seebeck coefficient of platinum.

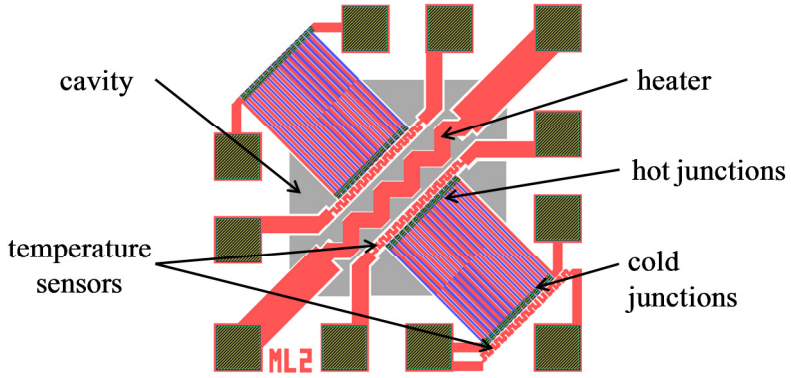

Figure 11. CASE test structure for Seebeck coefficient measurement.

The Seebeck coefficient, of highly doped n-SiC is about -10 µV/K at 300K. This Seebeck value for the 9×1020 doping level is 200 times lower than the report data from 2009 (using 1×1020 nitrogen doping) .While there is some expectation that the Seebeck coefficient would reduce (the Seebeck coefficient, is inversely proportional to the density of electrons, and higher doping concentration yields a smaller coefficient) -10 µV/K is much too low for high performance thermocouples and the SiC thermal conductivity is still too high. We could re-visit lower doping levels in the SiC to achieve large Seebeck coefficient but the large thermal conductivity (360 W/mK) make high thermal isolation difficult and near radiative limited performance difficult to achieve. The lower doped SiC based thermocouple is useful for an ambient air packaged detector (such as an ear thermometer) since the Seebeck coefficient and ZT is high. Poly-Si based thermocouples are better in vacuum packaged thermopile systems where near radiative limited performance is desired. A result of the Phase I SiC study was to shift the advanced thermocouple/thermopile research to poly-SiGe since poly-SiGe offers comparable electrical resistivity and Seebeck coefficient to poly-Si but thermal conductivity is reduced about 3-5 x (resulting in higher figure of merit, ZT) and the poly-Si thermopile allows a design to achieve near radiative limited performance when vacuum packaged.

3. N+/P+ Poly-SiGe thermocouple/thermopile:

The Phase I STTR research indicated that SiC was not a suitable material for vacuum packaged thermopiles where near radiative limited performance is desired for maximum system

performance. BFE and CASE determined that poly-SiGe was a suitable material choice for a higher performance option to the baseline poly-Si thermopile.

Poly-SiGe is a CMOS foundry compatible material and offers increased performance compared to conventional poly-Si gates in CMOS transistors. The CMOS advantage is the adjustable work function of poly-SiGe gates (adjusted with Ge content) and increased current drive capability in the PMOS transistor (as shown in figure 12)[ref4]. It is anticipated that poly-SiGe will be available at low cost in the future at CMOS foundries and available now at MEMS and custom IC process facilities.

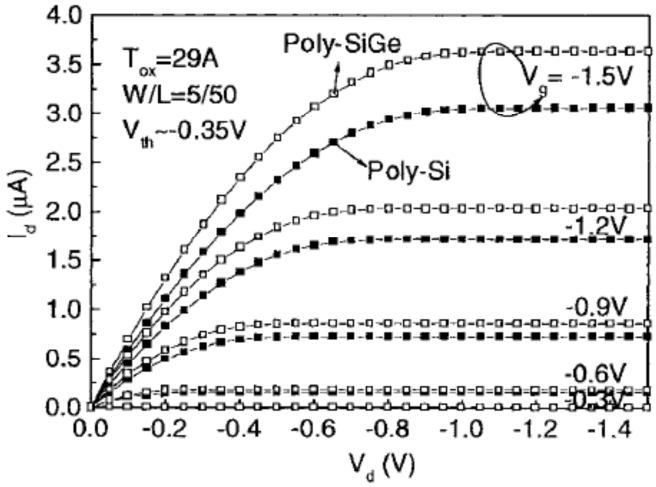

Figure 12. Poly-SiGe gate offers improved PMOS performance
(Lee, IEEE ELEC. DEV. LETT., VOL. 20, NO. 5, MAY 1999)[ref4]

The thermal conductivity of poly-SiGe depends on its stoichiometry and with about 30% germanium content, the phonon scattering effect reaches its maximum and thermal conductivity minimized. The poly-$Si_{0.7}Ge_{0.3}$ material properties has been reported in the literature for use in thermoelectric applications (Wijngaards and Wolffenbuttel, IEEE Trans. Electron Devices 52 pp. 1015–25, 2005)[ref5]. Table II shows a comparison of poly-Si and poly-SiGe thermoelectric properties. The thermocouple Seebeck coefficients and electrical resistivity is similar between poly-Si and poly-SiGe with the poly-SiGe exhibiting ~4-6 x reduction in the thermal conductivity. The figure of merit, ZT, for this data (@ 300K), shows poly-SiGe thermocouples having about 4x FOM advantage over poly-Si. Since poly-SiGe is less developed, this FOM advantage could most likely be improved with some poly-SiGe deposition and doping optimization.

Table II. Comparison of poly-Si and poly-SiGe materials (ref 1 and ref 5)

Material	Seebeck (α) (μV/K)	Elec. Resistivity (Ω x μm)	Thermal Cond. (W/m.K)	FOM (ZT) @ 300K
N+ Poly-Si	-140	12.0	33.1	0.015
P+ Poly-Si	160	20.0	30.6	0.013
N+ Poly-SiGe	-179	29.2	5.1	0.064
P+ Poly-SiGe	131	28.9	4.7	0.038

The poly-SiGe exhibits a TCR of ~ -2 μV/K^2 (~ 0.12%/K) and + 1 μV/K^2 (~ 0.08%/K) for the N+ and P+ materials shown in Table II. While this is not as good as poly-Si, it is considerably better than BiSb (0.31 %/K).

BFE envisions CASE fabricating a poly-SiGe thermopile on the Phase II effort similar to BFE's poly-Si thermopile fabricated in a CMOS foundry. The main difference would be the use of 2 μm design rules at CASE versus 0.18/0.25 μm design rules in a CMOS foundry. The 2 μm CASE photo-lithography design rule is not a disadvantage for large pixel size thermopiles (0.5 mm x 1.5 mm) that are wire bonded to BFE ROICs.

The poly-Si thermopile array will be processed in a CMOS foundry and have the option of including the readout circuitry on the same wafer and connected to the array for low cost and size. While the poly-Si thermopile meets the STTR topic goals, the advantage of a second approach, with poly-SiGe, offering even higher performance is a worthwhile goal. The poly-SiGe could be introduced into a commercial process facility when the technology is demonstrated. The poly-SiGe CMOS process could be also be processed at custom CMOS facilities such as SVTC Technologies.

4. Poly-Si and Poly-SiGe Thermopile Design:

Thermal detector response is proportional to the amount of energy in the absorbed photon flux, whereas photon detector response is proportional to the number of absorbed photons. A thermal detector comprises three distinct parts: An IR absorber, a temperature sensor (transducer) and thermal isolation, as illustrated in figure 13. The purpose of the IR absorber is to convert IR electromagnetic energy into heat energy. The thermal isolation, modulated by the thermal mass (heat capacity), converts the heat energy to a temperature change. The transducer converts the temperature change to a change in a measurable (usually electrical) parameter. The three parts of a thermal detector can be functionally independent, although may be designed in such a manner that they are interdependent. In the case of thermocouples the thermal isolation from support legs is part of the transducer.

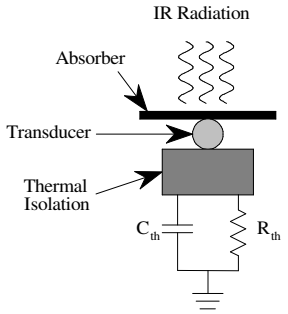

Figure 13. Constituent parts of a thermal detector (from Charles Hanson, L-3)

The voltage responsivity of a thermal detector is

$$R = \frac{\alpha_{abs}}{G_{th}} \left(\frac{dV}{dT} \right) \frac{1}{\sqrt{1 + \omega^2 \tau_{th}^2}} \ , \qquad (1)$$

where α_{abs} is the absorptivity (absorption efficiency),
G_{th} is the thermal conductance ($G_{th} = 1/R_{th}$),

(dV/dT) is the (voltage) response of the detector material per unit temperature change,
ω is the angular frequency of modulation of the signal.
τ_{th} is the thermal time constant.

Thermal detector and readout integrated circuit (ROIC) noise comes from a variety of sources including Johnson (or thermal) noise, current noise (typically 1/f), and temperature-fluctuation noise.

Temperature-fluctuation noise from the thermal detector is the random variation of the detector temperature resulting from the random exchange of heat with the environment. The spectrum of this variation is given by

$$\overline{\delta T(\omega)}^2 = \frac{4k_B T^2}{G_{th}} \frac{1}{1+\omega^2\tau_{th}^2} \ . \qquad (2)$$

This noise is band limited by the thermal time constant in the same manner as the responsivity. When integrated, the net temperature fluctuation is

$$\delta T = \sqrt{\frac{k_B T^2}{C_{th}}} \ , \qquad (3)$$

where C_{th} is the heat capacity ($\tau_{th} = R_{th}\, C_{th} = C_{th} / G_{th}$). The resulting output noise voltage is then

$$v = \left(\frac{dV}{dT}\right)\sqrt{\frac{k_B T^2}{C_{th}}} \ , \qquad (4)$$

and the noise-equivalent power (NEP) at low frequency is

$$NEP = \frac{G_{th}}{\alpha_{abs}}\sqrt{\frac{k_B T_d^2}{C_{th}}} = \frac{1}{\alpha_{abs}}\sqrt{\frac{k_B G_{th} T_d^2}{\tau_{th}}} \ . \qquad (5)$$

The noise-equivalent temperature difference (NETD) used as a figure of merit in thermal imagers is

$$NETD = \frac{4F^2}{A_d(\partial W/\partial T)_{\Delta\lambda}\tau_{opt}} NEP = \frac{4F^2}{A_d(\partial W/\partial T)_{\Delta\lambda}\tau_{opt}\alpha_{abs}}\sqrt{\frac{k_B G_{th} T_d^2}{\tau_{th}}} \ , \qquad (6)$$

where F is the optical *f*/number,
$(\partial W/\partial T)_{\Delta\lambda}$ is the blackbody differential emittance, and
τ_{opt} is the optical transmissivity.

Achieving the radiative limit for low NEP:

The rate of heat exchange between a thermal detector and its environment is

$$W = G_{cond}(T_d - T_b) + \sigma_B(T_d^4 - T_b^4)A_d \ , \qquad (7)$$

where G_{cond} is the mechanical thermal conductance,
σ_B is the Stefan-Boltzmann constant, and
T_b is the background/ambient temperature
A_d is the detector active area.

The second term in Eq. #7 is the radiation term. If radiation dominates, then the conductance is said to be radiation-limited, and the effective thermal conductance is

$$G_{rad} = \frac{dW}{dT_d} = 4\sigma_B T_d^3 A_d \ . \qquad (8)$$

The radiative thermal conductance of the ARMY STTR pixel is ~ 4.6 μW/K. In order to achieve radiation limited performance, the thermal conductance of the thermopile legs and the support structure should be much less than that due to radiative exchange.

5. Thermal time constant challenges:

The thermal time constant is related to the pixel heat capacity and thermal conductance as follows:

$$\tau_{th} = \frac{C_{th}}{G_{th}} \ . \qquad (9)$$

The heat capacity must be reduced concomitantly with the thermal conductance, in order to maintain a useful time constant. The heat capacity is given by

$$C_{th} = \rho c_p A_d z_d \ , \qquad (10)$$

where ρ is the average density of the pixel,
c_p is the average specific heat,
A_d is the detector physical area, and
z_d is the average detector thickness.

Using these two equations (9 and 10) with a total conductance twice Eq. #8 as an estimate, we get

$$\tau_{th} = \frac{\rho c_p z_d}{8\sigma_B T_d^3} \ . \qquad (11)$$

The only physical parameter in this equation is z_d; so this places a constraint upon the thickness of the detector (and absorber) structure. A time constant of 35 msec (from the STTR requirement: table I) dictates that the supported and thermally isolated structure thickness be only 150 nm, assuming an average c_p of 3.0 J/cm^2. Within this thickness the pixel must also contain an IR absorption structure. Low mass broadband absorbers combined with diffractive resonance and perforations in the structure will allow a thicker absorber layer while achieving low NEP and thermal time constant.

6. Thermal time constant reduction:

In the past ten years bolometer-based infrared imagers have been optimized for moving platforms or targets where image blur caused by a slow thermal time constant is a performance limitation. The desired thermal time constant is now less than 10 msec at the same time that thermal conductance is decreasing (required to reduce NETD). Perforated absorbers have been utilized to reduce thermal mass while maintaining high absorption.

Metal mesh absorption properties where analyzed in 1967 by Ulrich (Infrared Physics, Vol. 7, pp. 37-55, 1967). The perforated structure, with small holes compared to incident wavelength, can allow reduction in A_d (detector physical area) to reduce thermal mass (heat capacity) without reduction in IR absorption. The periodicity (pitch) of the holes can also provide diffractive resonance that provides even higher absorption and a method of spectral absorption tuning. In the case of thermopiles, using a front side access silicon etch, the absorber perforations also provide silicon etch access holes. In the case of a mesh, the equivalent electrical conductance is reduced, such that the absorber sheet resistance needs to be reduced from 377 Ω/□ for maximum absorption (depending on mesh dimensions as shown in figure 14). The absorption does not change rapidly with sheet resistance so a range of 150-300 Ω/□ is acceptable).

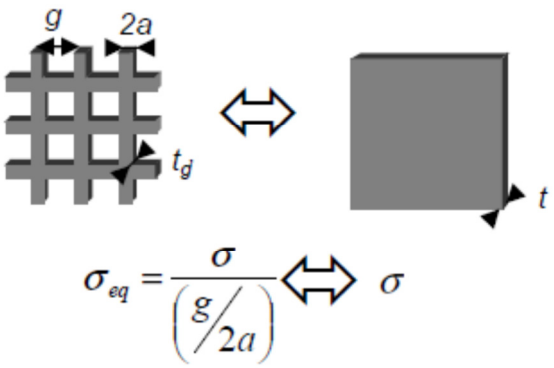

Figure 14. Mesh equivalent electrical conductivity

7. Absorber construction with a standard CMOS:

In the 180/250 nm CMOS structure (4-6 levels of metal/oxides) there is a significant amount of oxide between the metal layers as shown in the figure 15. In order to achieve <35 msec thermal time constant (STTR specification) in vacuum and with high thermal isolation the amount of silicon dioxide and other materials on the suspended platform needs to be reduced and all CMOS metals removed (thick metal reflects IR). The last step in the CMOS process will be to coat the wafers with photoresist and open up a region over the thermopile absorber and thermocouple legs for final etch. The area over the absorber is shown just prior to etch in figure 16. Metals M1-M6 are not used in the suspended thermopile region.

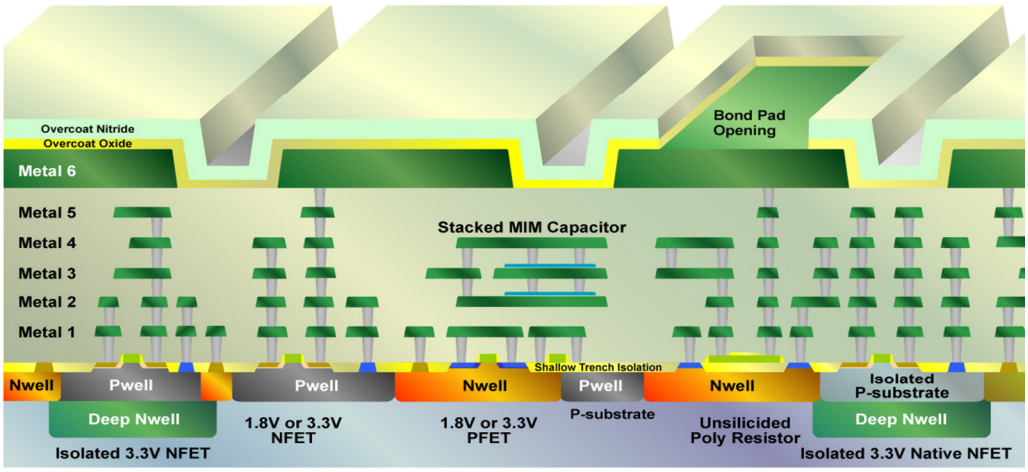

Figure 15. CMOS cross-section

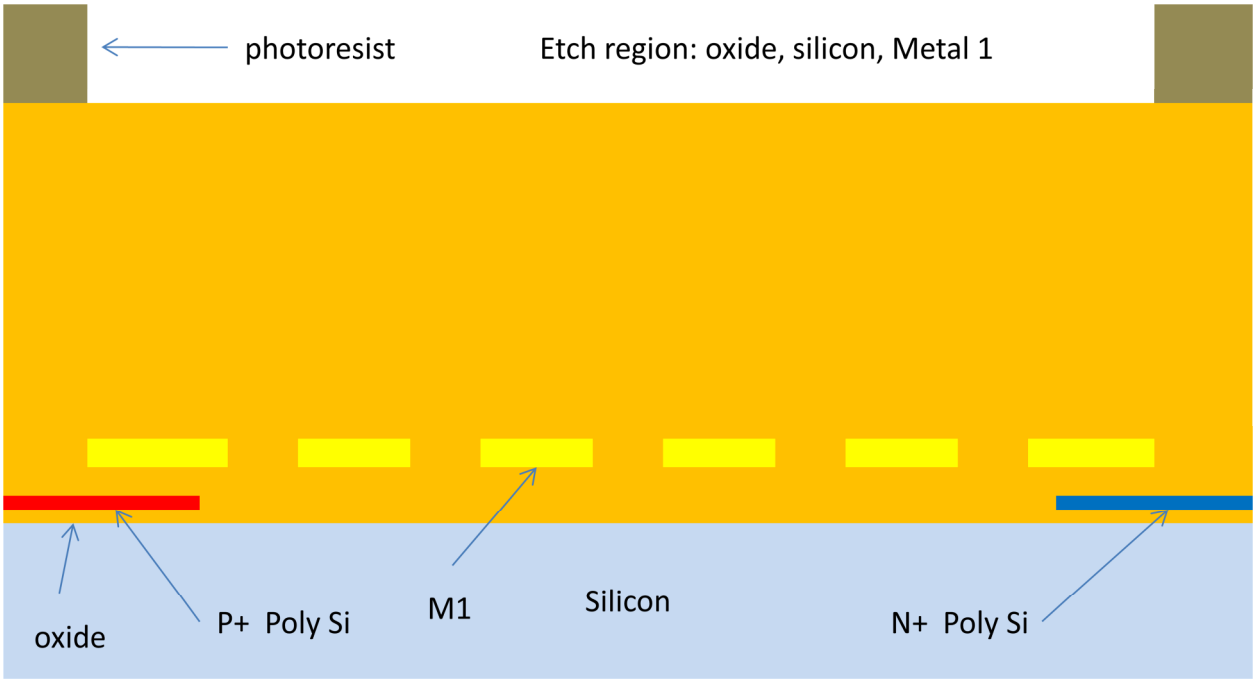

Figure 16. Thermopile absorber region prior to final etch

The structure in figure 16 uses metal M1 as an etch aperture for etching oxide and silicon. Figure 17 shows the thermopile absorption structure after etch (including M1) and photoresist removal. The etch sequence is: anisotropic (vertical direction) oxide etch, isotropic (all directions) dry XeF2 silicon etch, M1 aluminum etch, and finally oxygen plasma resist etch (oxygen plasma strip). The 600 nm thick oxide absorber does absorb portions of the LWIR but is not optimum for broadband IR absorbers.

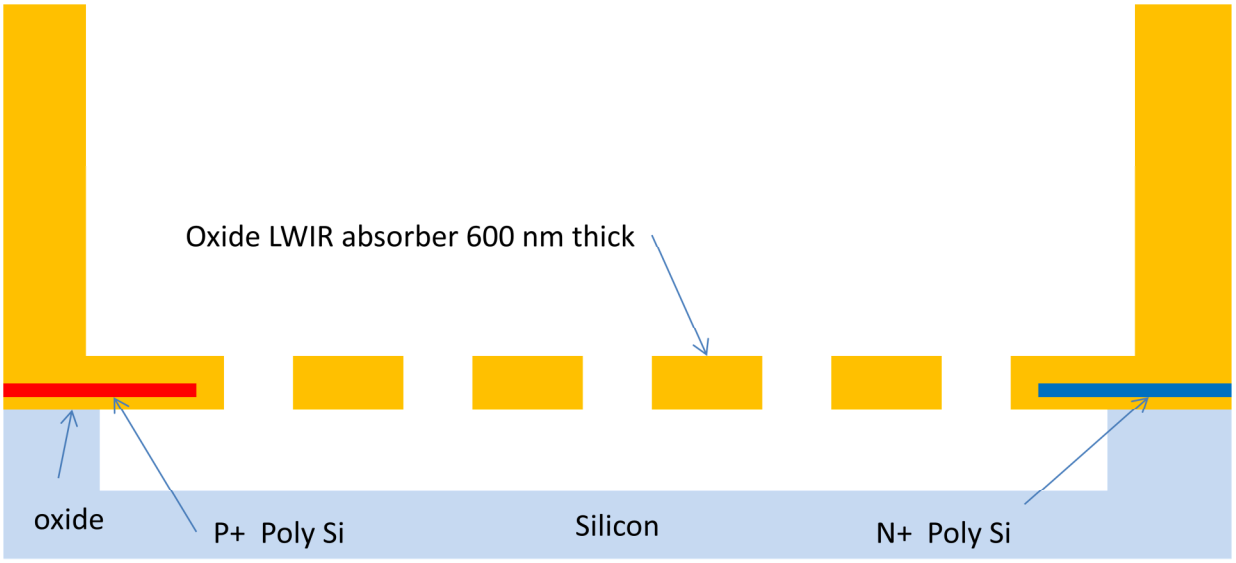

Figure 17. Thermopile suspended oxide absorber region after final etch

During the Phase I STTR research BFE determined that incorporating P+ polysilicon into the absorber structure, thus creating a resistive mesh less than 300 Ω/□ , results in a broadband IR structure that is compatible with standard CMOS processing and requires only one post CMOS etch step. Figure 18 shows a cross-section of the perforated polysilicon resonant absorber with P+ and N+ polysilicon thermocouple legs (TCs).

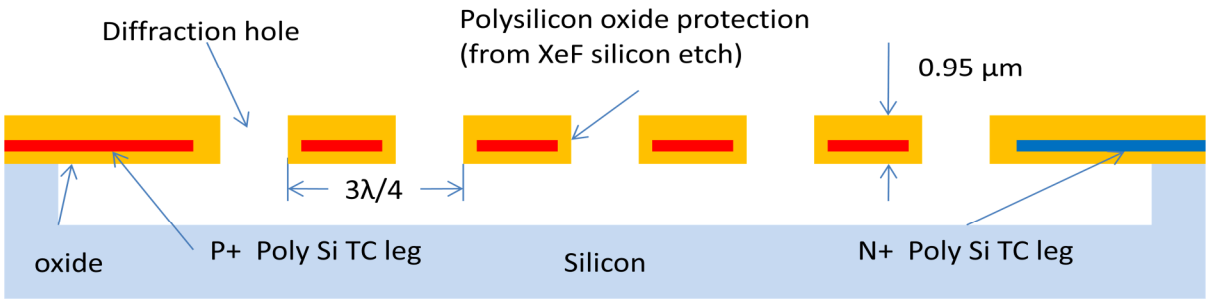

Figure 18. BFE STTR baseline thermopile design with perforated P+ polysilicon absorber -standard CMOS process and design rules (ITAR controlled process if required)

The sheet resistivity of the CMOS gate polysilicon is about 250-300 Ω/□ and is in an appropriate range for good polysilicon thermocouple performance and broadband infrared absorption. The thickness of the suspended structure is about 950 nm (200 nm field oxide, 250 nm poly-Si and 500 nm oxide on top of the poly-Si). The M1 etch aperture (shown in figure 16) is selected to leave some oxide on the sides of the poly-Si (this is required to prevent poly-Si etching with the XeF2 isotropic plasma silicon etch).

The perforations in the supported membrane allows an increase in absorption by diffractive resonance. The perforated absorber mesh pitch can be designed for a λ/4 or 3λ/4 distance (shown on figure 18) to maximize absorption at a particular wavelength λ. The diffractive resonance is somewhat broadband so does not have to be precise. On a linear spectrometer array the mesh pitch can be varied to cover the entire LWIR or even 2-16 microns to maximize absorption and reduce thermal mass. Note than the suspended structure is relatively thick (950 nm), but the perforations allows thermal mass reduction and attainment of a < 35 msec time constant).

8. Perforated IR absorber performance:

A group in Taiwan has made a thermopile (Al to P+ polysilicon thermocouples) with a perforated LWIR absorption structure as shown in figure 19.

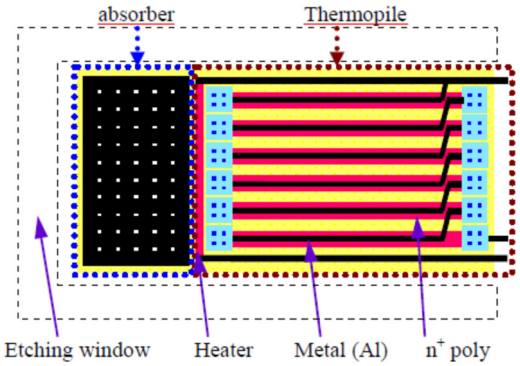

Figure 19. Perforated absorber (IEEE Sensors Conference 2010, paper A2P-Q12)

The perforated absorber structure is sometimes referred to as a "photonic crystal". A cross-section of the Taiwan thermopile (and absorber) is shown in figure 20. This process uses a 350 nm TSMC CMOS with 4-level metal. The final oxide in the absorber is ~ 5 μm thick (too much thermal mass for a vacuum encapsulated thermopile with fast response). Three perforation structures, figure 21, were investigated (honeycomb: H, square: S, rectangular: R and output signal, figure 22, compared to no perforations (WPC: without photonic crystal). The signal level is improved about 2x-4x for the perforated structures compared to no perforations. This data, from Taiwan, indicates that properly designed perforations can reduce absorber thermal mass and increase absorption compared to a uniform absorber layer.

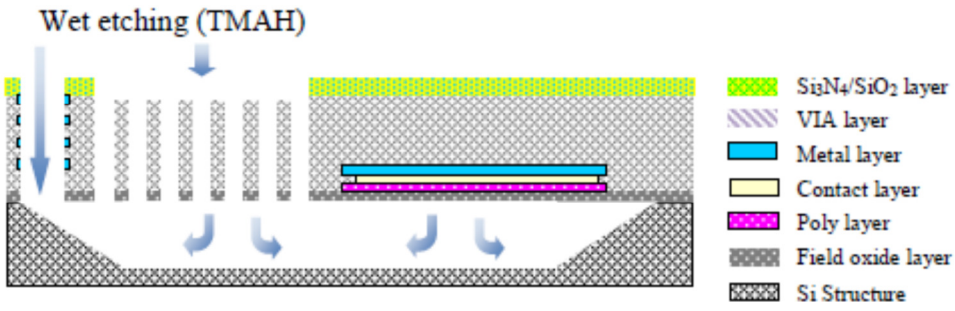

Figure 20. Cross-section of Taiwan absorber/thermocouple

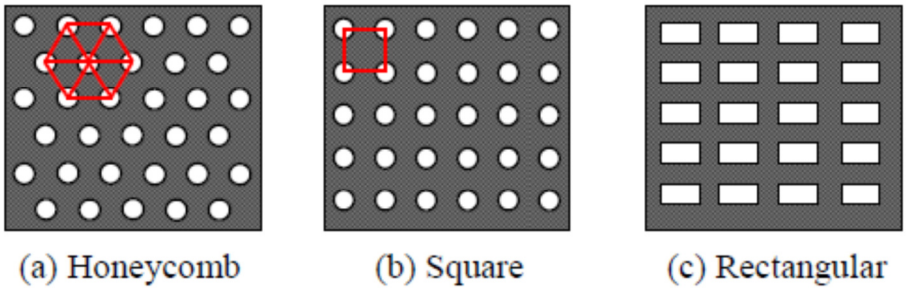

Figure 21. Photonic crystal perforation top view

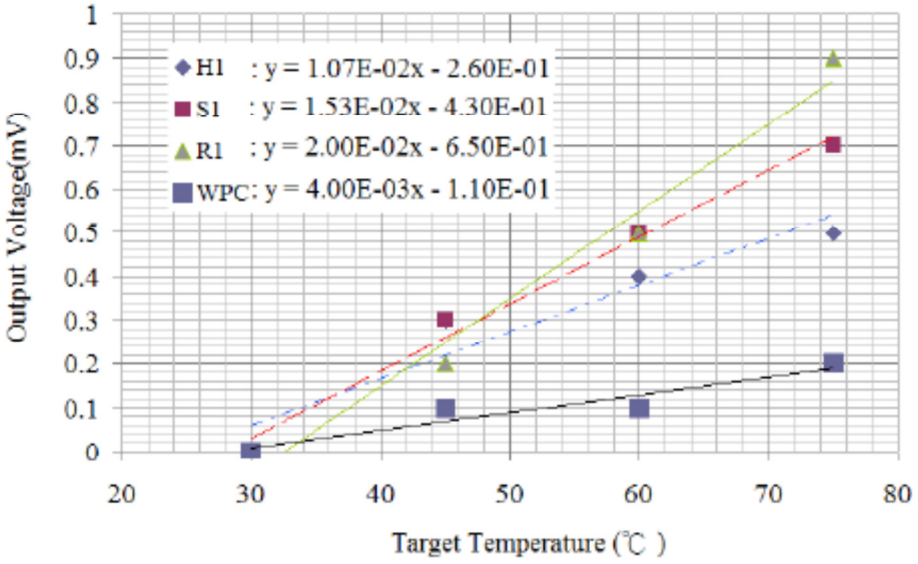

Figure 22. Output signal comparison (H, S, R and no perforations (WPC))

9. Phase I Thermopile Design and Performance:

BFE/CASE Phase II Design Approach Summary:

1. Use M1 aluminum metal layer to provide etch aperture for absorber mesh structure and silicon undercut. Keep about 200 nm oxide on polysilicon sidewalls.

2. Absorber membrane consists of 200 nm oxide below the 250 nm thick polysilicon and 500 nm thick oxide thickness on top of doped polysilicon (standard P+ polysilicon sheet resistance ~ 250- 300 Ω/□).

3. Designed for ~30 msec thermal time constant with ~50% mesh fill factor but effectively 100% area absorption (use diffractive resonance tuning to further improve absorption)

4. Total 0.5 mm x 1.5 mm absorber area thermal capacity ~ 0.8 E-6 J/K (using 50% absorber area perforations for additional diffractive resonance)

5. Thermopile leg total thermal conductance design goal ~ 2.21 E-5 W/K (to meet thermal time constant goals).

6. G_{th} ~ 5.8 x G_{rad}, (G_{rad} = 4.6 E-6 W/K) so NEP ~ 2.4x best possible for T_{th} = 30 msec.

7. Design compatible with 180/250 nm CMOS (ITAR compliant if required). The thermopile design can be processed with the BFE custom ROIC to eliminate wire bonds.

8. May require one additional masking steps at the end of the readout integrated circuit (ROIC) process in production (protect ROIC circuitry from thermopile oxide etch)- but still foundry compatible (thermopile array can be integrated with CMOS readout).

9. Poly-Si thermocouple legs and absorber layer, shown in figure 18, can be replaced with poly-SiGe for higher performance; however poly-SiGe not supported at CMOS foundry at this time. The poly-SiGe thermopile will require a custom process at CASE Western Reserve and array wire bonded to the BFE CMOS ROIC on Phase II.

10. The poly-SiGe material is similar to poly-Si (Seebeck coefficient and electrical resistivity). The poly-SiGe thermal conductivity is 4-5 x lower than poly-Si. This lower thermal conductivity allow widening of the poly-SiGe thermocouple legs (by 2x for 5 squares length - see figure 2) and this reduces thermocouple resistance by 50% allowing a doubling of the number of thermocouples in the poly-SiGe thermopile compared to poly-Si. The total thermal conductivity of the poly-Si and poly-SiGe is about the same (similar time constant and thermal isolation).

11. Utilize on wafer vacuum dewar for low cost in production but not on the Phase II effort.

10. Phase I thermopile design and performance prediction:

Table III shows the Phase I STTR linear array properties and predicted performance. The poly-Si thermopile array is processed in a CMOS foundry and the poly-SiGe array processed at CASE. Both arrays will be tested with existing BFE ROIC circuitry.

TABLE III. PHASE I LINEAR ARRAY PROPERTIES AND PREDICTED PERFORMANCE

Thermopile Property	Poly-Si Linear Array	Poly-SiGe Linear Array
Linear array pixels	≥1 x 64 (butted 1x32 arrays)	1 x 64
Operating wavelength	8-14 µm (2-16 µm option)	8-14 µm
# junctions per pixel	18	36
Junction type	N+/P+ poly-Si (~300 Ω/□)	N+/P+ poly-Si (~300 Ω/□)
Pixel Resistance	~162 KΩ	~162 KΩ
Leg Resistance	~ 4.5 KΩ (15 □ length)	~2.25 KΩ (7.5 □ length)
Thermal Conductance	~2.86x10^{-5} W/K(legs + Grad)	~2.86x10^{-5} W/K (legs + Grad)
Seebeck Coefficient	~300 µV/K (per thermocouple)	~300 µV/K (per thermocouple)
Pixel IR Absorption	> 80% pixel mesh tuning	> 80% pixel mesh tuning
Pixel width	0.49 mm	0.49 mm
Pixel height	1.5 mm	1.5 mm
Pixel pitch	0.5 mm	0.5 mm
Responsivity in vacuum	~300 V/W (2x gain at pixel)	~600 V/W (2x gain at pixel)
Johnson noise (23C, 30Hz, 162 kΩ)	0.40 µV RMS (with 60Hz bandwidth from chopper	0.40 µV RMS (with 60Hz bandwidth from chopper
D* (cmHz$^{1/2}$/W)	~ 7.55 x 10^{8}	~ 1.6 x 10^{9}
NEP (pW/Hz$^{1/2}$)	~43	~43
Response time (msec)	~30	~30
TCR (responsivity)	~0.04%/K	~0.08%/K
Thermopile processing	180 or 250 nm CMOS process	1 or 2 µm IC process
Thermopile Readout	BFE ROIC (on wafer)	BFE ROIC (wire bonded)
Vacuum packaging	On-wafer in production	Conventional package

THERMOPILE STRUCTURE

Figure 22 shows a top view of two thermopiles arrayed vertically. Each thermopile has two bonds pads as utilized by the BFE low noise chopper amplifier. The bond pads are located on the CMOS field oxide. The vertical separation shown between the two thermopiles is not accurately depicted and can be < 5 µm if desired. The electrical connection between the left and right side thermocouples is accomplished by low resistance polycide (~ 10 Ω/□ sheet resistance). The P+ and N+ thermocouple legs are made from heavily doped polysilicon (about 300 Ω/□ sheet resistance). The P+ polysilicon is also shown perforated in the IR absorber regions to create a broadband absorber of low thermal mass. The perforation pitch is 3λ/4 spacing (pitch) to provide absorption tuning by diffraction. The tuning can go as low as 2 µm wavelength (by 1.5 µm mesh pitch). The use of λ/4 pitch tuning is also possible if desired for more narrow band tuning, if desired, using feature size compatible with submicron CMOS (0.5 µm - 2.5 µm mesh pitch for 2-10 µm wavelengths).

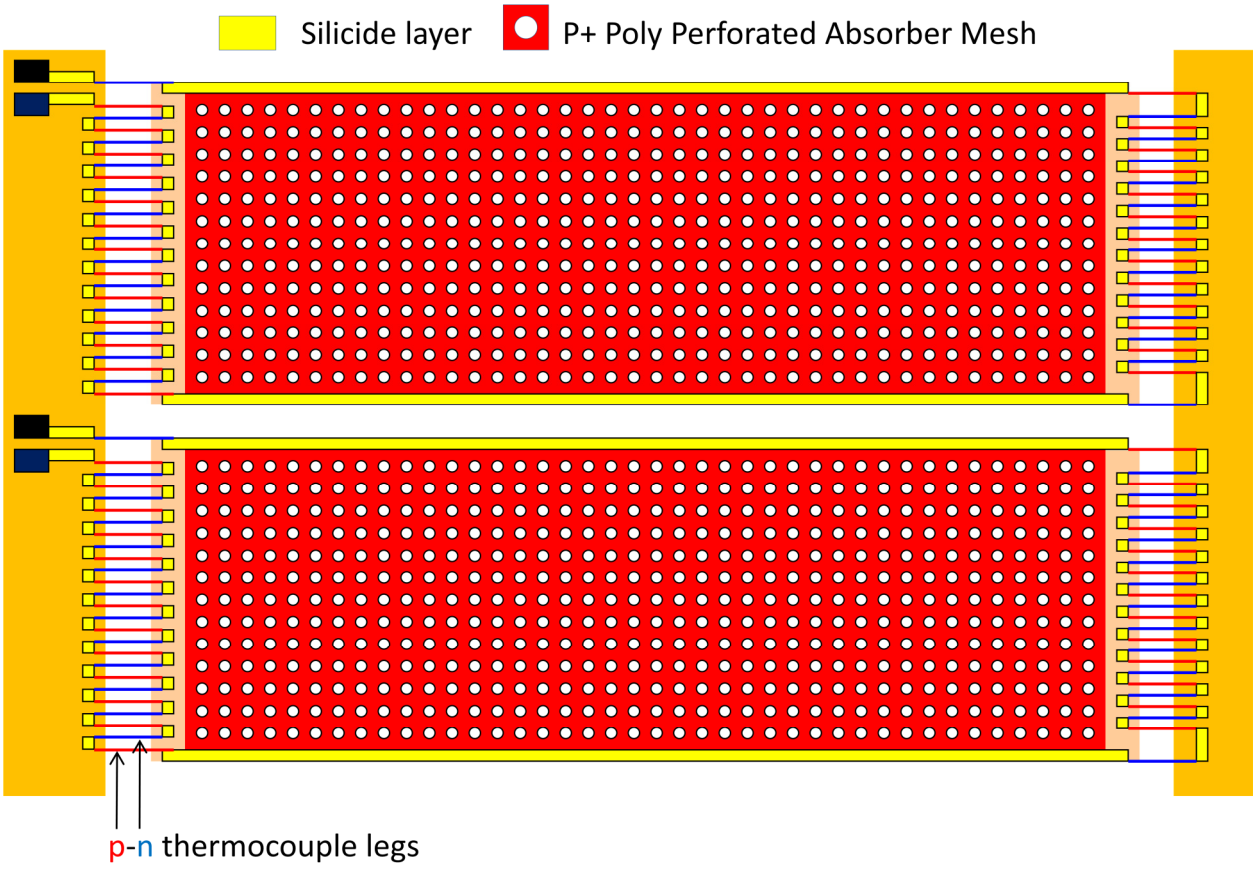

Figure 22. BFE Thermopile Top View (2x1 array)

The thermopile suspended membrane (thermocouples and absorber) is composed of three layers (200 nm thermal field oxide, 250 nm polysilicon and 500 nm deposited oxide). The total suspended platform thickness is 950 nm and provides a low thermal mass for fast thermal time constant with high thermal isolation. The P+ absorber mesh perforation further reduces thermal mass and provides uniform heat spreading across the suspended absorber platform. Most of the thermal conductivity (from hot to cold junctions) is a result of the polysilicon material. While

not shown in figure 22, the polysilicon legs are protected by a thin oxide to prevent etch during the silicon thermal isolation etch.

11. Phononic Crystal to reduce thermocouple leg thermal conductivity:

Numerous techniques for modifying the propagation of phonons are available, such as surface scattering, grain boundary/impurity scattering, and nano-structured materials like nanowires and nano-meshes. Phononic crystals composed of a periodic arrangement of scattering centers embedded in a homogeneous background matrix with a small lattice spacing on the order of the acoustic wavelength. This photonic mesh patterning results in a controllable redistribution of the phononic density of states and reduction in thermal conductivity of materials. This technique can be used to increase ZT and improved thermoelectric performance as discussed in reference 6.

Reference 6: Ihab El-Kady et. al., "Manipulation of Thermal Phonons: A Phononic Crystal Route to High-ZT Thermoelectrics," Photonic and Phononic Properties of Engineered Nanostructures, Proc. of SPIE Vol. 7946, 794615 · © 2011 SPIE.

Figure 23 shows a phononic crystal structured used the legs of a thermocouple. 180 nm x 180 nm holes are etched into the polysilicon leg on a 360 nm pitch.

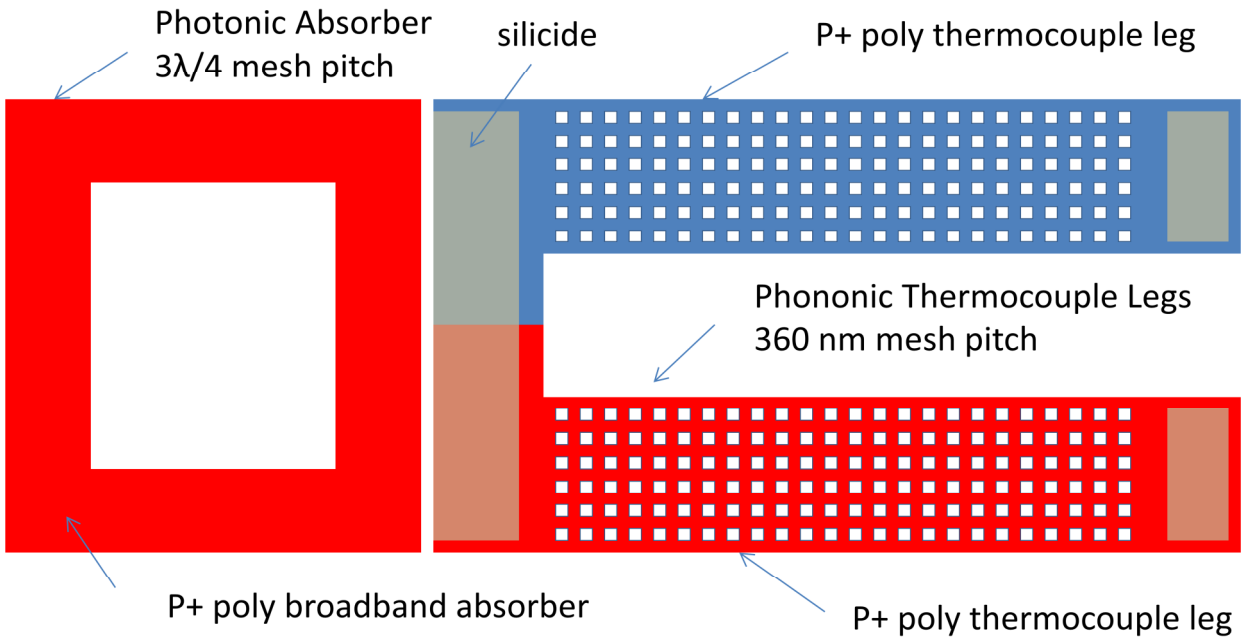

Figure 23. Thermocouple legs with photonic mesh to reduce thermal conductivity

In principle, the thermal conductivity and the electrical conductivity may be independently optimized in semiconducting nano-structures because different length scales are associated with phonons (which carry heat) and electric charges (which carry current). Phonons are scattered at surfaces and interfaces, so thermal conductivity generally decreases as the surface-to-volume ratio increases. In contrast electrical conductivity is less sensitive to a decrease in nanostructure
size.

A photonic crystal is an approach to independently control thermal conductivity based on altering the phonon band structure of a semiconductor thin film through the formation of a phononic nano-mesh film. These films are patterned with periodic spacing that are comparable to, or shorter than, the phonon mean free path. A nano-mesh fabricated with CMOS design rules of 250 nm or less may allow reduction of leg thermal conductivity while maintaining electrical resistivity (when width is adjusted to compensate for the mesh sheet resistance reduction). The thermal conductivity will exhibit further reduction as smaller design rules are utilized (≤ 180 nm). The performance analysis documented in Table III has not assumed use of a leg nano-mesh; however such structures can be easily incorporated into the thermopile structure if significant thermal conductivity is achieved. The goal is to achieve thermal conductivity reduction due to the behavior of the periodic nano-mesh lattice rather than a result of removing polysilicon and replacing it with air or silicon dioxide (of lower thermal conductivity).

Phase I Research Conclusion

Silicon-based semiconductor thermoelectric materials and integrated circuit (IC) process fabrication of thermopile linear arrays will be low cost and meet ARMY SSTR requirements. The Phase I design has the following advantages:

1. Poly-Si and poly-SiGe thermocouples offer a high Seebeck coefficient and low TCR.

2. Absorber structures using photonic micro-mesh reduce thermal mass.

3. Absorber micro-mesh pitch can be adjusted to tune wavelength of absorption

4. Thermocouple legs can use a phononic nano-mesh to further lower thermal conductance

5. IC processes provide large wafers and batch processing to lower fabrication cost.

6. Monolithic integration of the thermopile and (ROIC) on the same wafer is possible if desired.

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